TITLE

PIXEL STRUCTURE

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to a pixel structure, and more particularly to a pixel structure of a transflective liquid crystal display (LCD).

Description of the Related Art

A pixel structure of a conventional transflective LCD has a reflective cell and a transmission cell. Unavoidably, the reflective cell has nearly double the phase difference of the transmission cell. Reduction of cell gap of the reflective cell to approach that of the transmission cell has been adopted in the past to address this issue. Fig. 9A shows a perspective diagram of a pixel structure of a conventional transflective LCD. The pixel structure includes a reflective cell 10 and a transmission cell 20. The reflective cell 10 has a reflective film 12 and a cell gap d1. The transmission cell 20 has a cell gap d2.

An equivalent circuit is shown in Fig 9B. The reflective cell 10 and transmission cell 20 are both coupled to a storage capacitor Cs and a TFT (thin-film-transistor) transistor T1. Thus, only one driving voltage can be supplied. The anti-inversion approach provides the cell gaps d1 and d2 with the same phase difference. The cell gaps d1 and d2 must be optimized to fit the LCD's operating mode, an approach that is difficult to adjust.

SUMMARY OF THE INVENTION

The present invention is directed to pixel structure with exact reflection and transmission of transflective LCD.

Accordingly, the present invention provides a pixel structure of transflective LCD disposed between a first data line and a second data line. The pixel structure comprises a reflective cell having a first transistor and a first reflective electrode, and a transmission cell having a second transistor and a transparent electrode. The first transistor comprises a gate coupled to a scan line, a source coupled to the first data line, and a drain coupled to the first reflective electrode, wherein the first transistor is covered by the first reflective electrode. The second transistor comprises a gate coupled to the scan line, a source coupled to the second data line, and a drain coupled to the transparent electrode, wherein the second transistor is covered by a second reflective electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, reference is made to a detailed description to be read in conjunction with the accompanying drawings, in which:

FIG. 1 is an equivalent circuit diagram showing the pixel structure of the present invention;

FIG. 2A is a schematic diagram showing the pixel structure of the present invention;

FIG. 2B is a layout of FIG. 2A;

FIG. 3A is a schematic diagram showing another pixel structure of the present invention;

FIG. 3B is a layout of FIG. 3A;

FIG. 3C shows another configuration of FIG. 3A;

FIG. 3D shows another configuration of FIG. 3A;

FIG. 4A is a schematic diagram showing another pixel structure of the present invention;

FIG. 4B is a layout of FIG. 4A;

FIG. 5A is a schematic diagram showing another pixel structure of the present invention;

FIG. 5B is a layout of FIG. 5A;

FIG. 6A is a schematic diagram showing another pixel structure of the present invention;

FIG. 6B is a layout of FIG. 6A;

FIG. 7A is a schematic diagram showing another pixel structure of the present invention;

FIG. 7B is a layout of FIG. 7A;

FIG. 8A shows another configuration of FIG. 6A;

FIG. 8B shows another configuration of FIG. 6A;

FIG. 9A is a cross-section of a conventional pixel structure;

FIG. 9B is an equivalent circuit diagram showing the conventional pixel structure.

DETAILED DESCRIPTION OF THE INVENTION

FIG. 1 is an equivalent circuit diagram showing the pixel structure of the present invention. The pixel structure comprises thin film transistors T1 and T2 and storage capacitors Cs1 and Cs2. The thin film transistors T1 and T2 control drive voltages of a reflective cell 10 and a transmission cell 20 respectively. The phase differences of the reflective cell 10 and transmission cell 20 are normalized by adjusting the

gamma correction curves but cell gaps, and reflection and transmission of the LCD are exact.

First Embodiment

FIG. 2A is a schematic diagram showing the pixel structure of the present invention, and FIG. 2B is a layout of FIG. 2A. The pixel structure having a reflective cell 10 and a transmission cell 20 is disposed between a first data line DL1 and a second data line DL2, the reflective cell 10 comprises a transistor T1 and a reflective electrode RL1, and the transmission cell 20 comprises a transistor T2 and a transparent electrode TL1.

A projection of the first data line DL1 acts as a source TS1 of the transistor T1. A drain TD1 of the transistor T1 is coupled to the reflective electrode RL1 by a plug PL1. A projection of the data line DL2 acts as a source TS2 of the transistor T2. A drain of the transistor T2 is coupled to the transparent electrode TL1 by a plug PL2. Two projections of a scan line act as gates TG1 and TG2 of the transistors T1 and T2 respectively.

The transistor T1 is covered by the reflective electrode RL1, and the transistor T2 is covered by a reflective electrode RL2 of another pixel structure. The transparent electrode TL1 is on the center of the reflective electrode RL2. Metal layers M1 and M2, acting as storage capacitors, are disposed under the plugs PL1 and PL2 respectively. In this invention, the transparent electrode TL1 can be formed by Indium Tin Oxide (ITO).

Second Embodiment

FIG. 3A is a schematic diagram showing another pixel structure of the present invention, and FIG. 3B is a layout

of FIG. 3A. The pixel structure having a reflective cell 10 and a transmission cell 20 is disposed between a first data line DL1 and a second data line DL2, the reflective cell 10 having a transistor T1 and a reflective electrode RL1, and the transmission cell 20 comprises a transistor T2 and a transparent electrode TL1.

The first data line DL1 has a projection acting as a source TS1 of the transistor T1. A drain TD1 of the transistor T1 is coupled to the reflective electrode RL1 by a plug PL1. A projection of the data line DL2 acts as a source TS2 of the transistor T2. A drain of the transistor T2 is coupled to the transparent electrode TL1 by a plug PL2. Two projections of a scan line act as gates TG1 and TG2 of the transistors T1 and T2 respectively.

Transistors T1 and T2 are covered by the reflective electrode RL1, and disposed on the reverse side of the transparent electrode TL1. Metal layers M1 and M2, acting as storage capacitors, are disposed under the plug PL1 and PL2 respectively.

FIGS. 3C and 3D show other configurations of the embodiment. The pixel structure having a reflective cell 10 and a transmission cell 20 is disposed between a first data line DL1 and a second data line DL2.

The reflective cell 10 comprises a transistor T1 and a reflective electrode RL1, and the transmission cell 20 comprises a transistor T2 and a transparent electrode TL1.

A projection of the first data line DL1 acts as a source TS1 of the transistor T1. A drain TD1 of the transistor T1 is coupled to the reflective electrode RL1 by a plug PL1. A projection of the data line DL2 acts as a source TS2 of the

transistor T2. A drain of the transistor T2 is coupled to the transparent electrode TL1 by a plug PL2. Two projections of a scan line act as gates TG1 and TG2 of the transistors T1 and T2 respectively.

The transistor T1 and T2 are covered by the reflective electrode RL1, and disposed on the reverse side of the transparent electrode TL1. A metal layer M0 acting as a storage capacitor is disposed under the drains TD1 and TD2 of the transistors T1 and T2 respectively.

Third Embodiment

FIG. 4A is a schematic diagram showing another pixel structure of the present invention, and FIG. 4B is a layout of FIG. 4A. The pixel structure having a reflective cell 10 and a transmission cell 20 is disposed between a first data line DL1 and a second data line DL2, the reflective cell 10 comprises a transistor T1 and a reflective electrode RL1, and the transmission cell 20 comprises a transistor T2 and a transparent electrode TL1.

A projection of the scan line GL1 acts as a gate TG1 of the transistor T1. Two projections of the data line DL1 act as sources TS1 and TS2 of the transistors T1 and T2 respectively. A drain TD1 of the transistor T1 is coupled to the reflective electrode RL1 by a plug PL1. A projection of the scan line GL2 acts as a gate TG2 of the transistor T2. A drain TD2 of the transistor T2 is coupled to the transparent electrode TL1 by a plug PL2.

The reflective electrode RL1 covers the transistor T1 and a transistor of another pixel structure, and a reflective electrode RL2 of another pixel structure covers the transistor T2. The transparent electrode TL1 is disposed between the

transistor T1 and T2. Metal layers M1 and M2, acting as storage capacitors, are disposed under the plugs PL1 and PL2 respectively.

Fourth Embodiment

FIG. 5A is a schematic diagram showing another pixel structure of the present invention, and FIG. 5B is a layout of FIG. 5A. The pixel structure having a reflective cell 10 and a transmission cell 20 is disposed between a first data line DL1 and a second data line DL2, the reflective cell 10 comprises a transistor T1 and a reflective electrode RL1, and the transmission cell 20 comprises a transistor T2 and a transparent electrode TL1.

A projection of the scan line GL1 acts as a gate TG1 of the transistor T1. Two projections of the data line DL1 act as sources TS1 and TS2 of the transistors T1 and T2 respectively. A drain TD1 of the transistor T1 is coupled to the reflective electrode RL1 by a plug PL1. A projection of the scan line GL2 acts as a gate TG2 of the transistor T2. A drain TD2 of the transistor T2 is coupled to the transparent electrode TL1 by a plug PL2.

The transistors T1 and T2 are covered by the reflective electrode RL1, and disposed on the reverse side of the transparent electrode TL1. Metal layers M1 and M2, acting as storage capacitors, are disposed under the plugs PL1 and PL2 respectively.

FIGS. 6A and 6B show other configurations of the embodiment. A pixel structure having a reflective cell 10 and a transmission cell 20 is disposed between a first data line DL1 and a second data line DL2. The transistors T1 and T2 are

covered by a reflective electrode RL1, and disposed on different sides under the transparent electrode.

FIGS. 7A and 7B show other configurations of the embodiment. A pixel structure having a reflective cell 10 and a transmission cell 20 is disposed between a first data line DL1 and a second data line DL2. The transistors T1 and T2 are covered by a reflective electrode RL1, disposed around a transparent electrode TL1. A metal layer M1 is disposed under a drain TD1 of the transistor T1, and extends to an underside of a drain TD2 of the transistor T2.

FIG. 8A shows another configuration of the embodiment. A pixel structure having a reflective cell and a transmission cell is disposed between data lines DL1 and DL2, wherein the data lines are bent. The transistors T1 and T2 are covered by a reflective electrode RL1. The reflective electrode RL1 is disposed around a transparent electrode TL1. A bent metal layer M0 is disposed under the drains TD1 and TD2 of the transistors T1 and T2.

FIG. 8B shows another configuration of the embodiment. A pixel structure having a reflective cell and a transmission cell is disposed between data lines DL1 and DL2, wherein the data lines are bent. The transistors T1 and T2 are covered by a reflective electrode RL1. The reflective electrode RL1 is disposed around a transparent electrode TL1. A metal layer M0 is disposed under the drains TD1 and TD2 of the transistors T1 and T2.

In the present invention, the transistors T1 and T2 of the pixel structure control the drive voltages of the reflective cell and the transmission cell respectively, the reflection

and transmission of the pixel structure are exact, such that the cell gaps do not have to adjust.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.